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(54) Method of obtaining high quality silicon dioxide passivation on silicon carbide

Verfahren zur Erzeugung von Silizium-Dioxid-Passivierung hoher Qualität auf Silizium-Carbid

Méthode pour obtenir une passivation de haute qualité à base de dioxyde de silicium sur du carbure de silicium

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DE-A- 4 009 837

- JOURNAL OF THE ELECTROCHEMICAL SOCIETY vol. 136, no. 2, February 1989, MANCHESTER, NEW HAMPSHIRE US pages 502 - 507 PALMOUR ET AL 'Dopant redistribution during thermal oxidation of monocrystalline Beta-SIC thin films'

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Description

[0001] The present invention relates to a method of passivating microelectronic structures and in particular relates to passivation of silicon carbide structures using silicon dioxide.

[0002] Silicon carbide (SiC) has a number of theoretical and practical advantages that make its use desirable in microelectronic devices. These advantages are fairly well known and include a wide band gap, a high breakdown field, high thermal conductivity, high electron drift velocity, excellent thermal stability, and excellent radiation resistance or "hardness." These advantages have been recognized and described thoroughly in the patent and nonpatent literature.

[0003] One of the chemical advantages of silicon carbide is its ability to form a stable and well understood oxide, namely silicon dioxide (SiO_2), that can be used to passivate silicon carbide structure and devices. As known to those familiar with electronic devices, an appropriate thermally-grown oxide passivation layer provides an associated advantageous oxide-semiconductor interface that largely eliminates the presence of dangling bonds (sometimes referred to as dangling valences) on the semiconductor surface, and thus largely eliminates the associated problems such as interface charges and traps.

[0004] There are, however, some problems that arise from silicon dioxide passivation on silicon carbide because of certain properties of silicon carbide. In particular, a common p-type dopant for silicon carbide is aluminum. Although aluminum gives the highest p-type conductivity in silicon carbide, it recently has been discovered that the presence of aluminum incorporated into the thermally grown oxide passivation layers on p-type silicon carbide tend to cause high fixed oxide charge and high trap density at the silicon dioxide-silicon carbide interface. If the aluminum concentration is sufficiently high (for example when an oxide is grown on p^+ silicon carbide) the resulting oxide can have very high leakage currents, rendering it disadvantageous or even useless for passivation or electrical isolation. This problem does not occur when passivating silicon with silicon dioxide because aluminum is not a common dopant for silicon.

[0005] As a result of these characteristics, when thermally grown oxides have been used to passivate structures such as mesa p^+n^- junctions in silicon carbide, the resulting devices tend to demonstrate excessive leakage currents in reverse bias at relatively high voltages (i.e., greater than 50 volts). This leakage current is apparently caused by the poor quality of the passivation on the p^+ side of the junction, causing what effectively amounts to a short circuit around the junction. In some p-channel MOSFETs (metal-oxide-semiconductor field effect transistor), the gate contact has been observed to short entirely through the oxide where it overlaps the p^+ source and drain wells.

[0006] Additionally, in n-channel MOSFETs, where the electrical integrity of the oxide layers over the aluminum doped p-type channel region are extremely important, the high interface trap density and fixed oxide charge tend to cause the transistors to have high threshold voltages, low transconductances, low channel mobilities at room temperature, and all of which properties tend to change dramatically with temperature. As these MOSFETs are heated, their behavior improves because the increasing density of thermally generated carriers tend to fill the interface traps.

[0007] Another problem that arises from the difference between silicon carbide and silicon is that carbon-oxygen compounds are generated by the oxidation of silicon carbide during passivation that are not generated during passivation of silicon. Although not known for certain, these carbon-oxygen species may have their own degrading effect on the electrical integrity of silicon dioxide layers grown on silicon carbide, possibly contributing to fixed oxide charge and premature electric breakdown or wear out.

[0008] Finally, earlier work has demonstrated that n-type dopants such as nitrogen tend to pile up severely during thermal oxidation of silicon carbide, resulting in an interfacial concentration more than ten times higher than the bulk of the material. Such dopant pile up could additionally have a profound effect on the electrical characteristics of devices such as MOSFETs.

[0009] Therefore, there exists the need to develop a method for passivating silicon carbide device structures advantageously with silicon dioxide while avoiding the aforementioned problems.

[0010] In the patent application EP-A-0 363 944 an isolation oxide layer is formed on SiC by oxidation of a n-type SiC epitaxial layer. In the document DE-A-3 434 727 is disclosed the formation of a MOS structure on a SiC substrate comprising the deposition of a sacrificial silicon thin film, for example by decomposition of silane, and the oxidation of the sacrificial silicon thin film to produce the oxide.

[0011] The present invention consists in a method of obtaining high quality passivation layers on aluminium-doped, p-type silicon carbide surfaces that have a lower leakage current than passivation layers produced by thermally oxidizing p-type silicon carbide, the method comprising depositing a layer of silicon dioxide of a desired thickness on an aluminium-doped p-type silicon carbide portion of a device structure and without oxidizing the p-type silicon carbide portion; and thereafter oxidizing the device structure and the deposited silicon dioxide portion of the device structure to slightly extend the interface between the silicon dioxide and the aluminium-doped p-type silicon carbide into the aluminium-doped p-type silicon carbide portion.

[0012] There can thus be obtained high quality passivation layers on silicon carbide surfaces, and their associated high quality oxide-semiconductor interfaces in which the oxide passivation layers are substantially free

of dopants and carbon-oxygen by-product species that would otherwise degrade the electrical integrity of the oxide layer.

[0013] The foregoing and other objects, advantages and features of the invention, and the manner in which the same are accomplished, will become more readily apparent upon consideration of the following detailed description of the invention taken in conjunction with the accompanying drawings which illustrate preferred and exemplary embodiments, and wherein:

Figure 1 is a plot of drain current-voltage characteristics of a 6H-SiC inversion-mode MOSFET at (a) 298K, (b) 473K, and (c) 673K;

Figure 2 is another plot of drain current-voltage characteristics for a 6H-SiC n-channel inversion-mode MOSFET showing the effects of reducing aluminum in the oxide and measured at (a) 298K, (b) 423K, and (c) 573K;

Figures 3(a) and 3(b) are the initial and final device structures for an n-channel planar MOSFET structure; and

Figures 4(a), (b), and (c) are progressive cross-sectional views of the processing methodology for a hi-lo IMPATT diode.

[0014] The present invention is a method of obtaining high quality passivation layers on silicon carbide surfaces.

[0015] The oxidizing step preferably comprises thermal oxidation of the device structure.

[0016] The preferred method of depositing a layer of silicon dioxide of a desired thickness on the silicon carbide portion comprises depositing the layer by chemical vapour deposition.

[0017] The silicon carbide portion preferably has a polytype selected from the 6H, 3C, 4H, 2H and 15R polytypes of silicon carbide.

[0018] The method of the invention can be used to produce a silicon carbide base device structure having passivation areas that are substantially free of the impurities normally associated with oxides grown on silicon carbide. The structure comprises a silicon carbide portion, and a thermally grown oxidation layer upon the silicon carbide portion, the oxidation layer being substantially free of aluminum and of carbon-oxygen by-products typically associated with thermal oxidation of silicon carbide. In the most preferred device structure, the oxidation layer has an aluminum dopant concentration of 3E17 (3×10^{-17} cm^{-3}) or less. As known to those familiar with silicon carbide and with microelectronic device structures, the silicon carbide portion of the device structure can be selected from substrates, epitaxial layers, mesa sidewalls, implanted or diffused wells, and any combination of these structural elements.

[0019] Figures 1 and 2, although not representing identical devices, demonstrate some of the advantages of the present invention. Figure 1 is a set of three plots of drain current versus drain voltage at selected gate voltages for a 6H-SiC inversion-mode MOSFET at temperatures of 298K, 473K, and 673K. The techniques of the present invention were not used in producing the MOSFET characterized by Figure 1, and Figure 1 is thus included for comparative purposes.

[0020] By way of such comparison, Figure 2 represents the same information as Figure 1 taken at 298K, 423K, and 573K in which an attempt was made to eliminate aluminum entirely from the oxide. This was first attempted on some planar MOSFETs fabricated on the Si-face of silicon carbide and utilizing ion implanted n^+ source and drain wells. By way of further comparison, the device of Figure 1 was produced using dry oxide techniques, while that of Figure 2 was produced by a wet oxide process. Furthermore, the p-channel of the Figure 2 device contained less aluminum than the p-channel of the Figure 1 device.

[0021] Appropriate techniques for producing bulk silicon carbide, epitaxial layers of silicon carbide, ion implantation of silicon carbide, and dry etching of silicon carbide are set forth in numerous prior patents. These include U.S. Patents Nos. 4,912,063; 4,912,064; 4,865,685; 4,866,005; and 5,087,576.

[0022] The major difference between the MOSFETs formed in the attempt to eliminate aluminum from the oxide and previous MOSFETs was the incorporation of a very thin layer of undoped 6H-SiC grown on top of the p-channel layer. The p-type layer was first grown and measured to have $p = 4.3 \times 10^{15}$ cm^{-3}. Next, an epitaxial layer of undoped silicon carbide only 37 nanometers (nm) thick ($n = 2\text{-}8 \times 10^{15}$ cm^{-3}) was grown on top. The purpose of including this layer is to consume it during oxidation so that the SiO_2/SiC interface stops at a point very close to the p-type material or only one or two monolayers into it.

[0023] After fabricating the devices and implanting the wells, the device wafers were oxidized in wet oxygen at 1200°C for 49 minutes, yielding an oxide thickness of 62 nanometers. Assuming an oxide consumption factor of 0.47, and the loss of about 6 nanometers in a previous reactive ion etching (RIE) step, this thickness would have brought the SiO_2/SiC interface to within about 2 nm of the p-type material. Although it could not be specifically confirmed whether such dimensions were really the case or whether the interface had aluminum present, it was certain that there was much less aluminum present in the oxide than in previous MOSFETs.

[0024] Figures 1 and 2 show the improvements provided by the invention in such devices. For the device characterized in Figure 1, the maximum transconductance was 0.25 millisiemens per millimeter (mS/mm) at a gate voltage of +24 volts (V). The on-current at a gate voltage of +16 V was 0.5 milliamps (mA). In the invention, and as indicated in Figure 2, the room temperature drain current at a gate voltage of 16 volts was 18.6 mA and the transconductance at that gate voltage was 2.8 mS/mm. The threshold voltage was about 1.9 volts,

which is much lower than the 9 to 12 volts obtained for the device in Figure 1. The channel mobility was measured to be about 46 cm^2/V-sec, and the subthreshold leakage current (gate voltage equals 0 volts) was 560 nanoamps (nA).

[0025] Figures 2(b) and 2(c) show the comparative operation of the device at higher temperatures. When the temperature was raised to 150°C, as shown in Figure 2(b), both the current and transconductance at a gate voltage of 16 volts increased to 29 mA and 3.6 mS/mm, and the threshold voltage decreased to about -0.2 volts. This trend continued up to 300°C, as shown in Figure 2(c). At this temperature, the current and transconductance at the gate voltage of 16 volts were 35 mA and 3.9 mS/mm, respectively. Although the threshold voltage of the device fell to -0.8 volts, the drain current at a gate voltage of 0 volts was only 47 microamps (μA). The channel mobility at 300°C decreased to about 43.5 cm^2/V-sec.

[0026] Figures 3 and 4 further illustrate the use of the invention and the resulting product.

[0027] Figure 3(a) shows a device precursor broadly designated at **10** formed of an n-type 6H-SiC substrate **11** and a p-type 6H epitaxial layer **12**. In accordance with a method differing from the present invention, and in preparation for passivation, a sacrificially undoped epitaxial layer ("epilayer") **13** is added upon the p-type epitaxial layer **12**.

[0028] After oxidation and further processing the finished device, again designated at **10** for the sake of consistency, is illustrated in Figure 3(b). Figure 3(b) again illustrates the n-type substrate **11** and p-type epitaxial layer **12**, but also shows respective n^+ implanted wells **14** and **15**, a metallic source contact **16**, a metallic drain contact **17**, and a metallic gate contact **18**. In preferred embodiments, the source and drain contacts **16,17** are formed of nickel and the gate contact **18** of molybdenum. The oxide layer **19** resulting from the oxidation of the undoped epitaxial layer **13**, is also illustrated in Figure 3(a). The oxide layer **19** is formed from the undoped layer **13** rather than from the p-type layer **12** to thus minimize the dopant concentration in the oxide and any associated problems.

[0029] Figure 4 shows the progressive formation of a mesa type IMPATT (impact avalanche transit time) device broadly designated at **20** and incorporating an improved method of oxidizing a sacrificial layer of silicon containing material. Figure 4(a) illustrates an n-type 6H SiC substrate **21**, an n-type epilayer **22**, a second n-type epilayer **23**, and a p-type epilayer **24**. In a typical embodiment, the first n-type epitaxial layer **22** has a carrier concentration of between about 2 and 3E16, the second n-type epitaxial layer **23** has a carrier concentration of about 7E17, and the p-type epitaxial layer has a carrier concentration of 5E18 or higher.

[0030] Figure 4(b) illustrates the same structure but with the addition of a thin layer of polysilicon **25** to both the mesa and rear portions of the device. The thin polysilicon layer **25** is, of course, the sacrificial layer referred to herein. As set forth earlier herein, in certain embodiments a thin boron-doped silicon carbide layer can be added between the polysilicon layer **25** and the surface or edges of the respective SiC layers **21**, **22**, **23** and **24**. The boron-doped layer should be thick enough to keep aluminum from the interface while otherwise remaining as thin as possible. An appropriate thickness presently appears to be between about 1 and 50 nm.

[0031] Figure 4(c) illustrates a completed device. The difference from Figure 4(b) is the consumption of the polysilicon layer on the mesa portion of the device to form the passivation oxide layer **26**. Again, the dopant concentration in the oxide layer **26** can be kept very low, particularly adjacent the heavily doped p-type epitaxial layer **24**. As set forth earlier, if the oxide layer **26** had a sufficient carrier concentration, a short circuit could occur between layers **24** and **23**, thus incapacitating the device.

[0032] To complete the device, Figure 4 also illustrates an ohmic contact **27** to the substrate, preferably formed of nickel, and an ohmic contact **28** to the p-type epitaxial layer on the mesa, and preferably formed of an aluminum alloy.

[0033] In the invention, the method comprises oxidizing a device structure formed of a layer of silicon dioxide of a desired thickness on a silicon carbide portion of the device structure to slightly extend the interface between the silicon dioxide and the silicon carbide into the silicon carbide portion. As in the prior art embodiments, the oxidizing step preferably comprises thermal oxidation of the device structure. The method of the invention further comprises the step of depositing the layer of silicon dioxide of a desired thickness on the silicon carbide portion of the device structure without oxidizing the silicon carbide portion prior to the step of oxidizing the overall device structure. In this regard, the preferred method of depositing a layer of silicon dioxide of a desired thickness on the silicon carbide portion comprises depositing the layer by chemical vapor deposition. As in the previous embodiment, the silicon carbide portion preferably has a polytype selected from the group consisting of the 6H, 3C, 4H, 2H and 15R polytypes of silicon carbide. Similarly, the invention has been found to be most useful when the step of depositing the layer of silicon dioxide comprises depositing the layer on an aluminum doped, p-type portion of silicon carbide.

[0034] It will be understood to those familiar with such devices that the invention can also be applied to structures in addition to those illustrated herein, including p-channel planar MOSFETs having implanted p-type wells, and those in which the p-type source and drain are formed from epilayers that have been partially etched away. In either case, an oxide typically will border both a p-portion and an n-portion of the device so that any leakage through the oxide portion will essentially short the device, the avoidance of which is one of the main advantages of the present invention.

[0035] The invention can also be applied to any vertical power MOSFET design in SiC, such as DDMOS (double diffused MOS), UMOS (U-channel MOS), or VMOS (V-channel MOS), that would require use of aluminum as the channel dopant.

Claims

1. A method of obtaining high quality passivation layers on aluminium-doped, p-type silicon carbide surfaces that have a lower leakage current than passivation layers produced by thermally oxidizing p-type silicon carbide, the method comprising:

   depositing a layer (13) of silicon dioxide of a desired thickness on an aluminium-doped p-type silicon carbide portion (12) of a device structure and without oxidizing the p-type silicon carbide portion; and thereafter;
   oxidizing the device structure (12) and the deposited silicon dioxide portion (13) of the device structure to slightly extend the interface between the silicon dioxide and the aluminium-doped p-type silicon carbide into the aluminium-doped p-type silicon carbide portion.

2. A method according to claim 1 wherein the step of oxidizing the device structure comprises thermally oxidizing the device structure.

3. A method according to claim 1 or claim 2 wherein the layer of silicon dioxide is deposited on the silicon carbide portion of the device by chemical vapour deposition.

4. A method according to any preceding claim wherein the silicon carbide portion has a polytype selected from the group consisting of the 6H, 3C, 4H, 2H and 15R polytypes of silicon carbide.

Patentansprüche

1. Verfahren zur Erzeugung von Passivierungsschichten hoher Qualität auf aluminiumdotierten Siliciumcarbidoberflächen vom p-Typ, die einen geringeren Verluststrom als Passivierungsschichten haben, welche durch thermische Oxidation von Siliciumcarbid vom p-Typ erzeugt werden, wobei das Verfahren darin besteht, daß man

   eine Schicht (13) von Siliciumdioxid einer erwünschten Dicke auf einem aluminiumdotierten Siliciumcarbidbereich vom p-Typ (12) einer Vorrichtung und ohne Oxidation des Siliciumcarbidbereiches vom p-Typ abscheidet und danach
   die Vorrichtung (12) und den abgeschiedenen Siliciumdioxidbereich (13) der Vorrichtung oxidiert, um die Grenzfläche zwischen dem Siliciumdioxid und dem aluminiumdotierten Siliciumcarbid vom p-Typ etwas in den aluminiumdotierten Siliciumcarbidbereich vom p-Typ zu erstrecken.

2. Verfahren nach Anspruch 1, bei dem die Stufe des Oxidierens der Vorrichtung thermisches Oxidieren der Vorrichtung umfaßt.

3. Verfahren nach Anspruch 1 oder 2, bei dem die Siliciumdioxidschicht auf dem Siliciumcarbidbereich der Vorrichtung durch chemische Abscheidung aus der Dampfphase abgeschieden wird.

4. Verfahren nach einem der vorausgehenden Ansprüche, bei dem der Siliciumcarbidbereich einen Polytyp hat, der aus der Gruppe ausgewählt ist, die aus den 6H-, 3C-, 4H-, 2H- und 15R-Polytypen von Siliciumcarbid besteht.

Revendications

1. Procédé pour obtenir des couches de passivation de haute qualité sur des surfaces en carbure de silicium du type p dopé à l'aluminium qui ont un courant de fuite plus faible que les couches de passivation produites en oxydant thermiquement du carbure de silicium du type p, le procédé comprenant les étapes de :

   - déposer une couche (13) de dioxyde de silicium d'une épaisseur souhaitée sur une partie en carbure de silicium de type p dopé à l'aluminium (12) d'une structure de dispositif et sans oxyder la partie de carbure de silicium de type p ; et ensuite ;
   - oxyder la structure de dispositif (12) et la partie de dioxyde de silicium déposé (13) de la structure du dispositif pour légèrement étendre l'interface entre le dioxyde de silicium et le carbure de silicium de type p dopé à l'aluminium dans la partie de carbure de silicium de type p dopé à l'aluminium.

2. Procédé selon la revendication 1, dans lequel l'étape d'oxyder la structure de dispositif comprend d'oxyder thermiquement la structure de dispositif.

3. Procédé selon la revendication 1 ou la revendication 2, dans lequel la couche de dioxyde de silicium est déposée sur la partie en carbure de silicium du dispositif par déposition en phase vapeur par procédé chimique.

4. Procédé selon l'une quelconque des revendications précédentes, dans lequel la partie en carbure de silicium comporte un polytype choisi à partir du groupe constitué des polytypes 6H, 3C, 4H, 2H et 15 R de carbure de silicium.

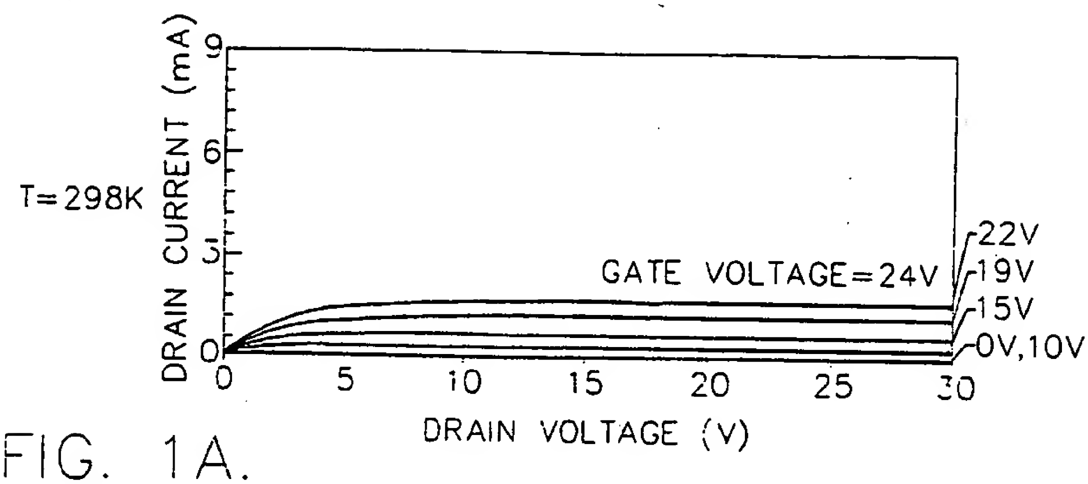

T=298K
DRAIN CURRENT (mA)
0
3
6
9
GATE VOLTAGE=24V
22V
19V
15V
0V,10V
0
5
10
15
20
25
30
DRAIN VOLTAGE (V)

FIG. 1A.

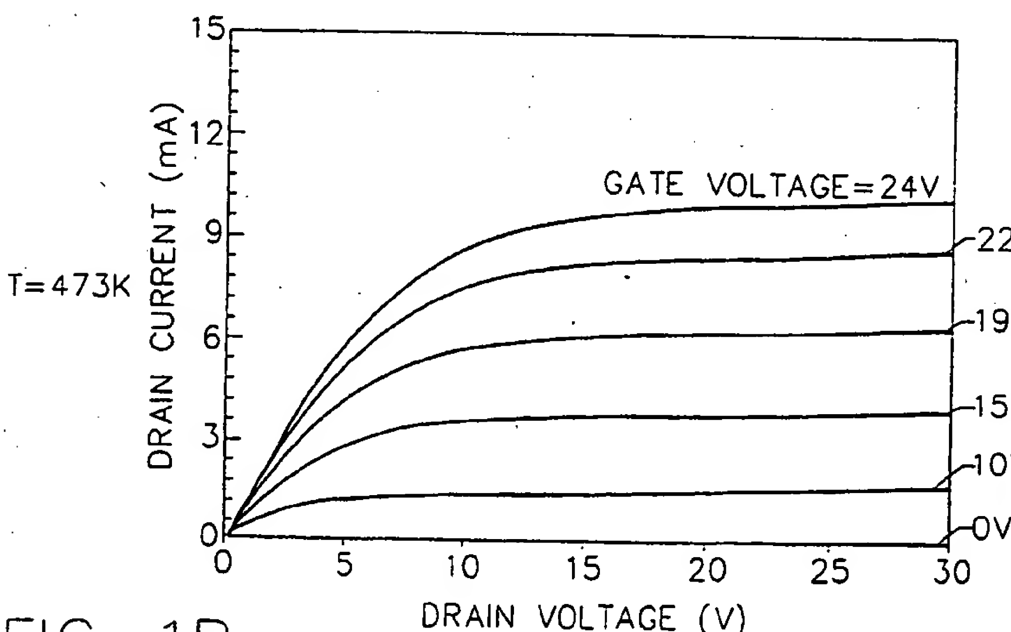

T=473K
DRAIN CURRENT (mA)
0
3
6
9
12
15
GATE VOLTAGE=24V
22V
19V
15V
10V
0V
0
5
10
15
20
25
30
DRAIN VOLTAGE (V)

FIG. 1B.

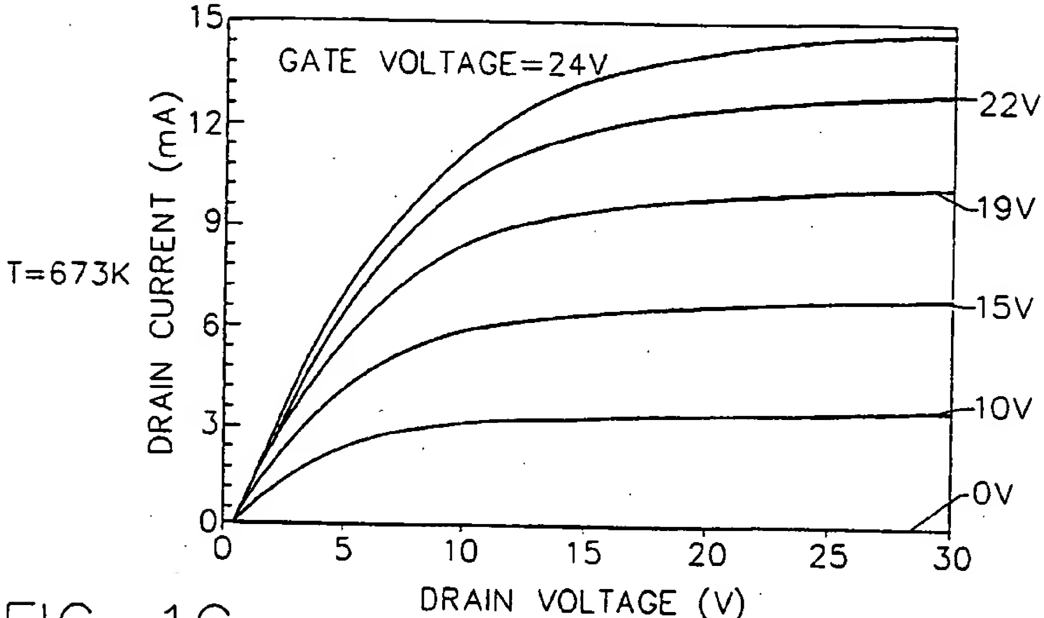

15
12
9
6
3
0
GATE VOLTAGE=24V
22V
19V
15V
10V
0V
T=673K
DRAIN CURRENT (mA)
0
5
10
15
20
25
30
DRAIN VOLTAGE (V)

FIG. 1C.

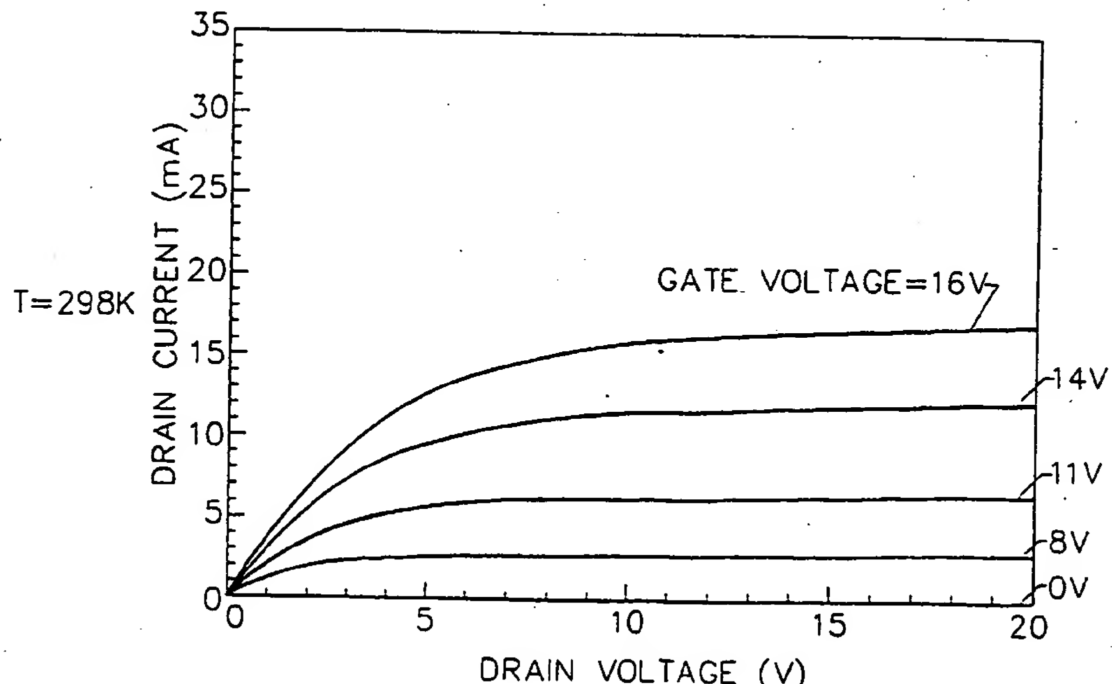
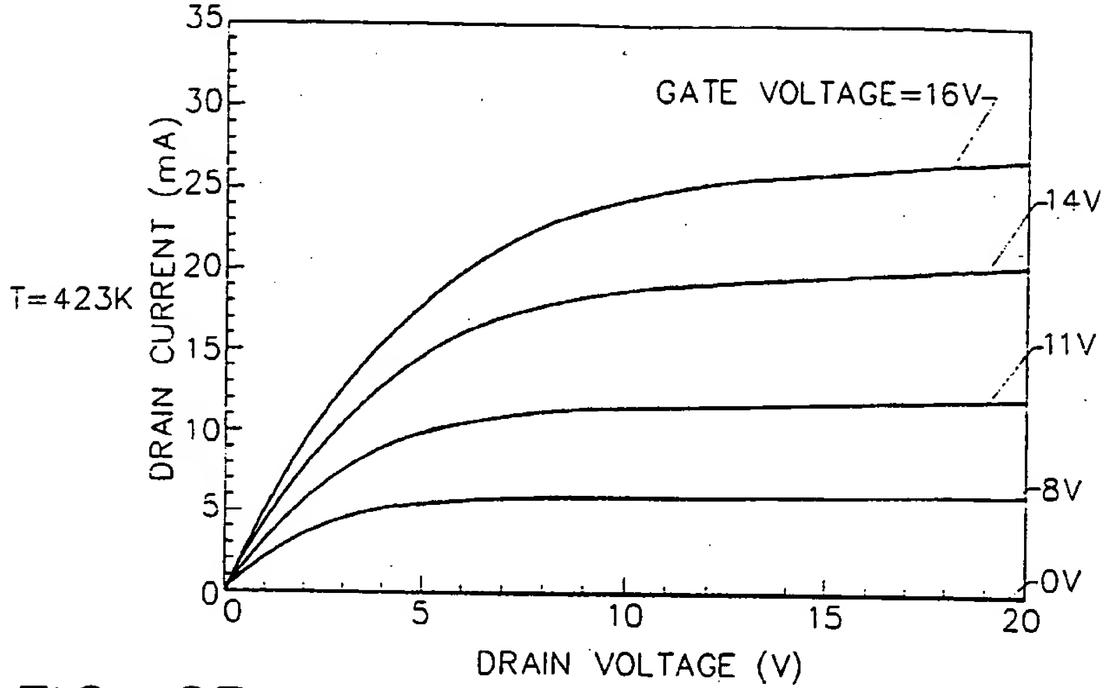
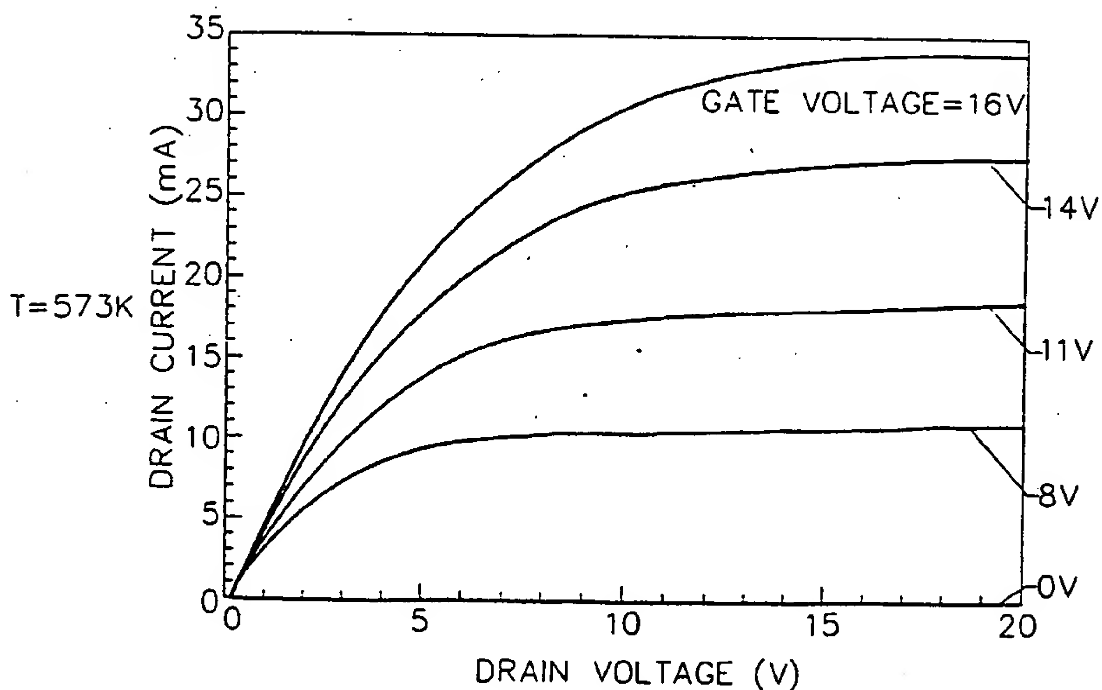

35
30
25
20
15
10
5
0
T=298K
DRAIN CURRENT (mA)
GATE VOLTAGE=16V
14V
11V
8V
0V
0
5
10
15
20
DRAIN VOLTAGE (V)

FIG. 2A.



35
30
25
20
15
10
5
0
DRAIN CURRENT (mA)
T=423K
GATE VOLTAGE=16V
14V
11V
8V
0V
0
5
10
15
20
DRAIN VOLTAGE (V)

FIG. 2B.



35
30
25
20
15
10
5
0
DRAIN CURRENT (mA)
T=573K
GATE VOLTAGE=16V
14V
11V
8V
0V
0
5
10
15
20
DRAIN VOLTAGE (V)

FIG. 2C.

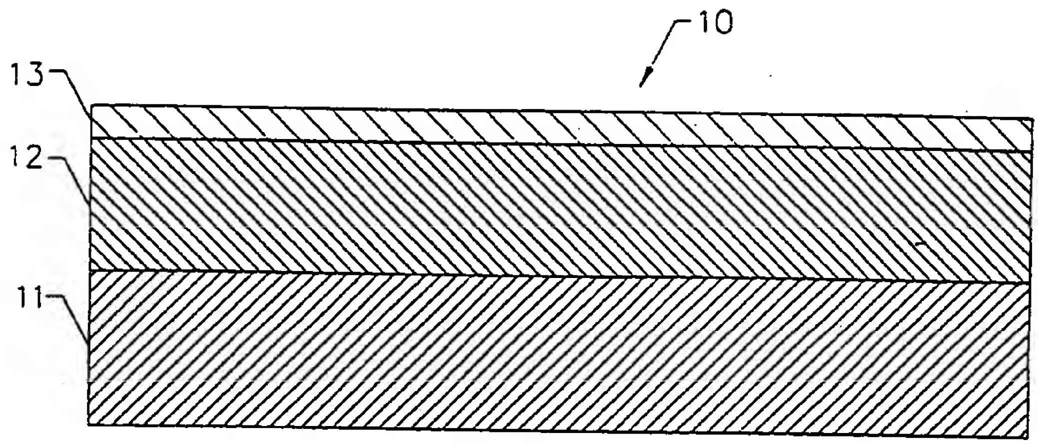


FIG. 3A.

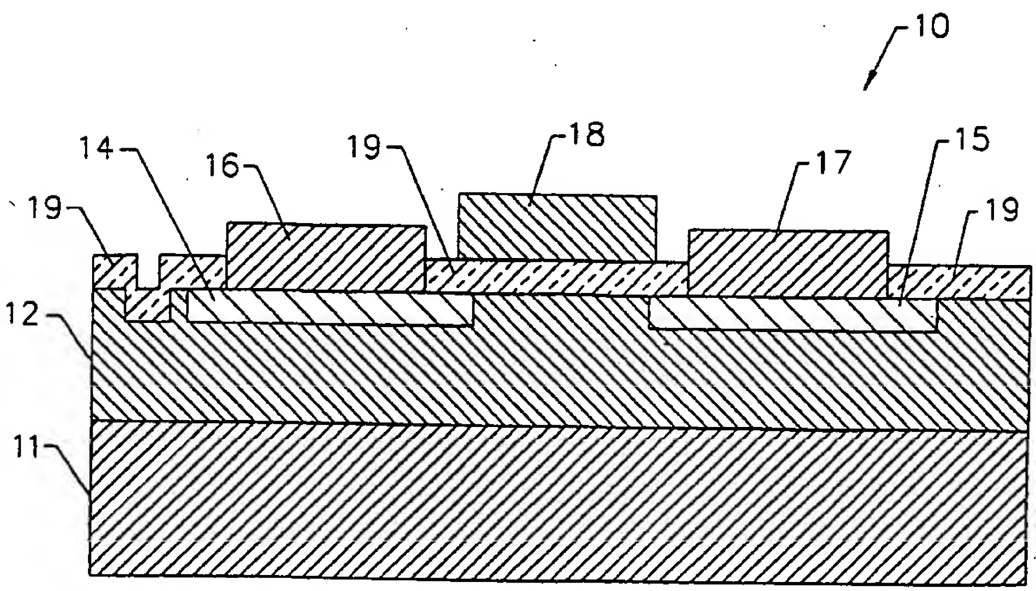


FIG. 3B.

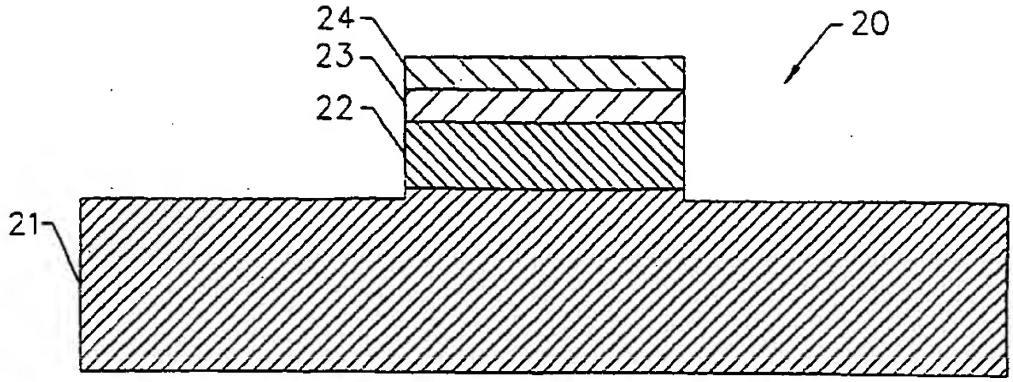


FIG. 4A.

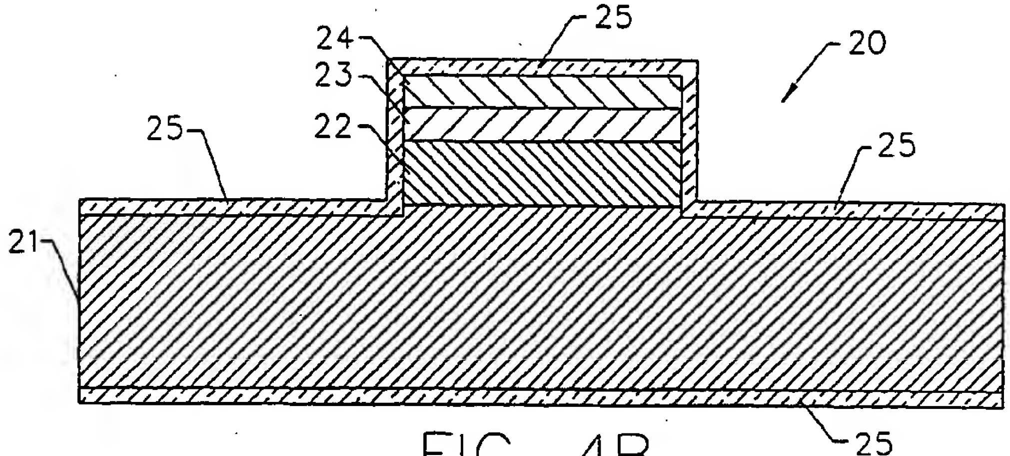


FIG. 4B.

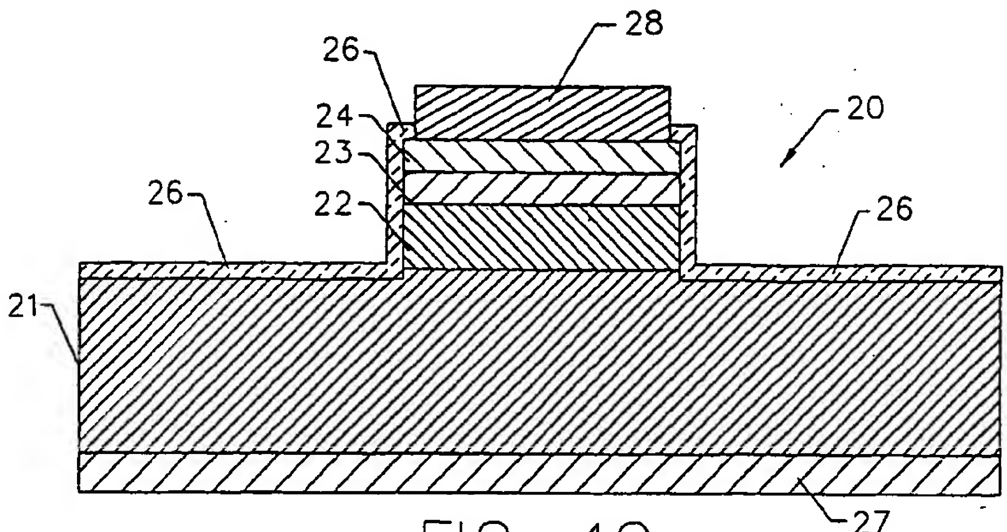


FIG. 4C.